REMARKS/ARGUMENTS

Reconsideration and allowance of the subject application are respectfully requested.

As an initial matter, filed with this response is a certified copy of the priority document. Acknowledgment of receipt of this certified document is respectfully requested.

In addition, Applicants submit an Information Disclosure Statement. The Examiner is requested to provide an initialed copy of the PTO-1449 form indicating consideration of these references with the next communication from the Patent Office. Applicants wish to bring to the Examiner's attention that U.S. Patent 6,331,856 has been listed because the equivalent Taiwanese Patent 337,570 has been cited in the Taiwanese application corresponding to the instant application.

Claim 6 stands rejected under 35 USC §112, second paragraph, with the Examiner noting insufficient antecedent basis for "said sum of absolute differences." Claim 6 now depends from claim 5 so that there is now antecedent basis. In addition, claims 1, 2, 3, 6 and 7 have been amended in a non-substantive way to recast certain method-type operations as apparatus configurations. None of these amendments is narrowing or is a surrender of any subject matter.

Claims 1, 11 and 12 stand rejected under 35 USC §103 as being unpatentable over U.S. Patent 5,025,407 to Gulley in view of U.S. Patent 4,317,168 to Messina. This rejection is respectfully traversed.

Gulley discloses a graphics floating point coprocessor 1200 designed to work in conjunction with a host graphic processor 120. The coprocessor performs arithmetic matrix calculations. With respect to the independent claims, the Examiner admits that Gulley fails to teach that the number of loaded data words loaded into the coprocessor depends on whether the start address of the operand data is aligned with a word boundary. Applicants agree that this is a deficiency with Gulley. But there is no need to even determine whether Messina remedies that deficiency or whether a person of ordinary skill in the art would have been properly motivated to modify Gulley using Messina's teachings as proposed by the Examiner. This is the case because Gulley also fails to disclose that the graphics coprocessor 1200 is

> responsive to a coprocessor load instruction on said main processor to load one or more loaded data words into said coprocessor and perform at least one coprocessor processing operation specified by said coprocessor load instruction using said one or more loaded data words to provide operand data to generate at least one result data word.

The Examiner refers to column 2, lines 3-10 which simply explain that coprocessors "[accept] from the host a set of operands and an instruction as to the operation to be performed on the operands." Where in this text is the coprocessor responsive to a coprocessor load instruction executed on the main processor?

To give the Examiner an example of such a coprocessor load instruction, the Examiner's attention is directed to the non-limiting example described in the specification on page 8, beginning at line 5. In this non-limiting example, special coprocessor load instructions (e.g., USALD instructions) are executed by the main

processor 8 that serve to load either two or three data words into the coprocessor 10. As explained beginning at line 20, the USALD instruction is passed (either directly or in the form of one or more control signals) to the coprocessor where it triggers the control and arithmetic function logic 24:

> "to control the loading of the required number of data words from either the cache 12 or the main memory 14 via the main processor 8 and then also carry out the sum of the absolute differences calculation using these loaded values and values from the coprocessor memory 18."

Because Gulley's coprocessor operates by accepting from the host a set of operands and an instruction as to the operation to be performed, Gulley requires a separate instruction to determine what operation is to be performed in the coprocessor. Such additional and separate instructions are not required for the present invention because the operation to be performed is determined by the coprocessor load instruction used to load the data words itself. By having the coprocessor load instruction also trigger the data processing operation to be performed by the coprocessor upon operands within the loaded data words to generate result data words, considerable advantages are achieved in terms of speed and code density.

Lacking features recited in claim 1, and with similar features recited in independent claims 11 and 12, it is respectfully submitted that the rejection of these claims is improper and should be withdrawn.

The Examiner makes additional rejections of the dependent claims based upon Gulley, Messina, and York (for claims 2-10), Gulley, Messina, and Langendorf (for

claim 8), and Gulley, Messina, and Wu (for claim 10). None of these tertiary references overcome the deficiencies of Gulley described above.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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